WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor device, comprising:

forming a polysilicon gate electrode over a substrate;

forming source/drain regions in said substrate proximate said polysilicon gate electrode;

forming a blocking layer over said source/drain regions, said blocking layer comprising a metal silicide;

siliciding said polysilicon gate electrode to form a silicided gate electrode.

2. The method as recited in Claim 1 wherein said forming a blocking layer occurs prior to said siliciding said polysilicon gate electrode.

3. The method as recited in Claim 1 wherein said blocking layer is a silicided source/drain contact region.

4. The method as recited in Claim 1 wherein said silicided gate electrode comprises a different metal silicide than said blocking layer.

5. The method as recited in Claim 4 wherein said blocking layer comprises a cobalt silicide and said silicided gate electrode comprises a nickel silicide.

6. The method as recited in Claim 1 wherein said blocking layer has a thickness ranging from about 10 nm to about 35 nm.

7. The method as recited in Claim 1 further including forming a protective layer over said polysilicon gate electrode prior to said forming a blocking layer over said source/drain regions.

8. The method as recited in Claim 7 wherein said protective layer is a silicon nitride protective layer.

9. The method as recited in Claim 1 wherein siliciding said polysilicon gate electrode to form a silicided gate electrode includes fully siliciding said polysilicon gate electrode to form a fully silicided gate electrode.

10. A method for manufacturing an integrated circuit, comprising:

forming semiconductor devices over a substrate, including;

forming a polysilicon gate electrode over a substrate;

forming source/drain regions in said substrate proximate said polysilicon gate electrode;

forming a blocking layer over said source/drain regions, said blocking layer comprising a metal silicide;

siliciding said polysilicon gate electrode to form a silicided gate electrode; and

forming interconnects within dielectric layers located over said substrate for electrically contacting said semiconductor devices.

11. The method as recited in Claim 10 wherein said forming a blocking layer occurs prior to said siliciding said polysilicon gate electrode.

12. The method as recited in Claim 10 wherein said blocking layer is a silicided source/drain contact region.

13. The method as recited in Claim 10 wherein said silicided gate electrode comprises a different metal silicide than said blocking layer.

14. The method as recited in Claim 13 wherein said blocking layer comprises a cobalt silicide and said silicided gate electrode comprises a nickel silicide.

15. The method as recited in Claim 10 wherein said blocking layer has a thickness ranging from about 10 nm to about 35 nm.

16. The method as recited in Claim 10 further including forming a protective layer over said polysilicon gate electrode prior to said forming a blocking layer over said source/drain regions.

17. The method as recited in Claim 16 wherein said protective layer is a silicon nitride protective layer.

18. The method as recited in Claim 10 wherein siliciding said polysilicon gate electrode to form a silicided gate electrode includes fully siliciding said polysilicon gate electrode to form a fully silicided gate electrode.